ROM coupled to the second bus.

11 10
27. (New) The mobile radiotelephony controller of Claim 26, wherein the first bus has a first width, the second bus has a second width, and the third bus has a third width; the first width is greater than the second width, and the second width is greater than the third width.

12 11
28. (New) The mobile radiotelephony controller of Claim 27, wherein the digital signal processor, the microcontroller, the DMA controller, the ROM, the first memory, and the second memory are all disposed on the same single integrated circuit.

REMARKS

This is in response to the Office Action of 18 March 2003. Claims 1-16 are pending in the application, and Claims 1-16 have been rejected.

By this amendment, a new title has been provided, Claims 1-16 have been cancelled, and new Claims 17-28 have been added.

No new matter has been added.

In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

About The Invention

The present invention relates generally to the integration of at least two processors onto a single integrated circuit, or chip, and providing a shared memory arrangement by which each of the at least two integrated processors are able to access various memories. More particularly, the present invention relates

to integrating a first and a second processor on an integrated circuit wherein the first processor accesses a first memory through at least one cache memory disposed intermediate the first memory and the first processor, and the at least one cache memory is coupled to the first memory via a first bus, and wherein the second processor is coupled to a second bus and accesses the first memory through a bridge that provides an appropriate interface between the first bus and the second bus, the busses being dissimilar. In various further aspects of the present invention, the first and second processors may operate at different clock frequencies; there may be a direct communication path between the first processor and the second processor; and there may be an additional cache memory disposed between the second processor and the second bus.

Title

The Examiner states that the title of the invention is not descriptive. The Examiner has required a new title that is clearly indicative of the invention to which the Claims are directed.

By this amendment the previous title has been replaced with a new title that is indicative of the invention to which the Claims are directed. More particularly, the new title (Memory Sharing Arrangement For An Integrated Multiprocessor System) clearly indicates that the claimed invention is directed to the relationship between memory and processors in an integrated multiprocessor system.

Applicant respectfully submits that this amendment satisfies the requirement set forth by the Examiner.

Rejections under 35 USC 112, second paragraph

Claims 1-16 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

By this amendment, Claims 1-16 have been cancelled. Applicants respectfully submit, that in view of this amendment, the rejections under 35 USC 112, second paragraph, have been rendered moot.

Rejections under 35 USC 102(e)

Claims 1-5, 9-12, and 16 have been rejected under 35 USC 102(e), as being anticipated by Nakagawa, et al., (US Patent 6,353,863).

By this amendment, Claims 1-5, 9-12, and 16 have been cancelled. Applicants respectfully submit, that in view of this amendment, the rejections under 35 USC 102(b) have been rendered moot.

Rejections under 35 USC 103(a)

Claims 6-8 and 13-15 have been rejected under 35 USC 103(a) as being unpatentable over various combinations of Nakagawa, et al., Elabd (US Patent 6,525,426) and Okummura, et al., (US Patent 5,974,493)

By this amendment, Claims 6-8 and 13-15 have been cancelled. Applicants respectfully submit, that in view of this amendment, the rejections under 35 USC 103(a) have been rendered moot.

New Claims 17-28

New Claims 17-28 are directed generally to an electronic product, and more particularly to a mobile radiotelephony controller. The claimed invention provides an integrated multiprocessor with a shared memory arrangement. A first processor accesses a first memory through a pair of caches that are disposed between the first processor and a first bus to which the first memory is coupled. A second processor accesses the first memory through a first bus

bridge which is disposed between a second bus, to which the second processor is coupled, and the first bus, to which the first memory is coupled. The bridge is used because the first and second busses are dissimilar. A second memory is accessed by the first processor through a second bridge that is disposed between a third bus of the first processor and the second bus, to which the second memory is coupled. As recited in the Claims, a DMA controller is coupled to the second bus to manage the transfer of data between the second memory and the first processor.

Support for these Claims can generally be found throughout the specification, and can more particularly be found at pages 5-6, and in Fig. 1.

Applicants respectfully submit that electronic product, as set forth by the Claims, does not appear to be disclosed or suggested in the references cited by the Examiner.

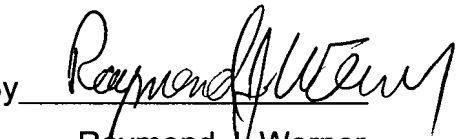
Conclusion

All of the rejections in the outstanding Office Action of 18 March 2003 have been responded to, and Applicants respectfully submit that the pending Claims 17-28 are now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

Dated: 16 May 2003
Portland, Oregon

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